

Intellectual Property Analysis of 3PAR, Inc. U.S. Patent No. RE40877

The Dell vs. Hewlett-Packard Bidding War for 3PAR, Inc.

September 3, 2010

Hewlett-Packard's \$33-a-share offer values 3Par at 325 times the company's earnings before interest, taxes, depreciation and amortization during the past year. In contrast, the median multiple over 21 computer-services deals in the past five years was 16.

Background

HP shareholders just purchased 3PAR and a whole bunch of over-priced intangible assets – in fact, they may be the proud owners of a ton of intellectual property liabilities.

The past month has been an exciting and eventful one for 3PAR, Inc. and its potential suitors, Dell and Hewlett-Packard. On August 16, 2010, Dell made an offer to acquire the data storage company for \$18 a share, for a total purchase price of \$1.15 billion. Unexpectedly, on August 23, Hewlett-Packard submitted an offer for 3PAR topping Dell's bid in the amount of \$24 a share, or \$1.5 billion. This event set off an old-fashioned back-and-forth bidding war which culminated in HP upping its offer to \$33 a share, \$2.4 billion total. HP's winning bid, \$1.15 billion more than the original offer from Dell, is almost a billion dollars in excess of HP's original bid.

In the balance lay one of the last independent high-end storage vendors and an opportunity to leverage 3PAR's technology and distribute it through large sales channels. Hewlett-Packard ended up paying more than three times 3PAR's \$9.65 per share closing price on August 13th, before Dell's bid for the company became public knowledge. Shaw Wu, an analyst for Kaufman Bros. in San Francisco, noted that HP seemed to be willing to bid for the asset at any price. The question remains, however; was this a good investment, or did HP overpay based on a value assumption that may or may not be supported by 3PAR's underlying technology?

Conspicuously, no market analyst began to handicap the patent litigation risk of having HP own 3PAR's intellectual property. 3PAR has played in a market that has a very different patent litigation profile when compared to HP. In their existing market, dubious patents lead to quiet settlements with parties knowing each others' weaknesses and not seeking to have their own dirty business aired.

3PAR has over 35 patents – all of which have been analyzed by M•CAM and are available in a limited edition M•CAM Triage™. An example is highlighted below.

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M•CAM has conducted an intellectual property analysis of 3PAR, Inc.'s U.S. Patent Reissue No. RE40877 to understand the strength and defensibility of the patent in the face of prior and concurrent art innovations. Using the M•CAM DOORS™ software platform, the innovation space surrounding RE40877 was examined to determine which patent or patents may provide alternatives to or alter the value of RE40877.

3PAR, Inc. patent selection:

<u>Document #</u>	<u>Title</u>	<u>Assignee Name</u>	<u>Priority</u>	<u>File</u>	<u>Issue</u>
US 6,973,484	Method of communicating data in an interconnect system	3PARdata, Inc.	29-Dec-00	29-Dec-00	6-Dec-05
USRE40877	Method of communicating data in an interconnect system	3PARdata, Inc.	29-Dec-00	10-Jul-08	18-Aug-09

Intellectual Property Analysis

Technology in RE40877

U.S. Pat. No. 6,973,484 was issued on December 6, 2005, and submitted for reexamination on July 10, 2008. On August 18, 2009, it was reissued as RE40877, without change. This application was related to the subject matter disclosed in U.S. patent application Ser. No. 09/633,088, entitled "Data Storage System," filed on August 4, 2000, now U.S. Pat. No. 6,658,478, and U.S. patent application Ser. No. 09/751,649, entitled "Communication Link Protocol Optimized for Storage Architectures", filed on December 29, 2000.

The RE40877 patent abstract reads as follows:

"A method is provided for communicating data in an interconnect system comprising a plurality of nodes. In one aspect, the method includes: issuing a command packet from a first node, the command packet comprising a respective header quadword and at least one respective data quadword for conveying a command to a second node, wherein the command is selected from a group comprising a direct memory access (DMA) command, an administrative write command, a memory copy write command, and a built in self test (BIST) command; receiving the command packet at the second node; issuing an acknowledgement packet from the second node, the acknowledgement packet comprising a respective header quadword for conveying an acknowledgement that the command packet has been received at the second node."

Using M•CAM DOORS™, several examples of un-cited prior art were identified that may limit the strength and breadth of the RE40877 patent claims. One such instance of precedent innovation, U.S. Pat. No. 5,864,738 held by Cray Inc., is of particular interest.

<u>Document #</u>	<u>Title</u>	<u>Assignee Name</u>	<u>Priority</u>	<u>File</u>	<u>Issue</u>
US 5,386,566	Inter-processor communication method for transmitting data and processor dependent information predetermined for a receiving process of another processor	Hitachi, Ltd.	20-Mar-91	18-Mar-92	31-Jan-95
US 6,073,211	Method and system for memory updates within a multiprocessor data processing system	International Business Machines Corporation	13-Dec-94	18-Apr-97	6-Jun-00
US 5,864,738	Massively parallel processing system using two data paths: one connecting router circuit to the interconnect network and the other connecting router circuit to I/O controller	Cray Research, Inc.	13-Mar-96	13-Mar-96	26-Jan-99

Excerpts from the claims of the RE40877 and Cray Inc.'s '566 patents are provided to illustrate the similarities in innovation in this technology space. Key similarities are shown in **bold**.

<i>Excerpt of claims from 3PAR, Inc. U.S. Patent No. RE40877</i>	<i>Excerpt of claims from Cray Inc. U.S. Patent No. 5,864,738</i>
<p>1. A method for communicating data in a data storage system, the data storage system comprising a plurality of interconnected nodes, each node having a respective cache memory comprising a plurality of cache lines, each cache line having the same predetermined size, the method comprising:</p> <p>providing new data for writing into a portion of a particular cache line in a memory region of a cache memory located at a local node, wherein data written to the memory region are mirrored to at least another memory region in at least another cache memory located at a remote node;</p> <p>reading out existing data from the particular cache line in the memory region of the cache memory located at the local node;</p> <p>merging the new data with the existing data;</p> <p>writing the merged data into the particular cache line in the memory region of the cache memory at the local node; and</p> <p>transferring the merged data over a communication link to the remote node for writing into said another memory region in said another cache memory located at the remote node.</p> <p>2. The method of claim 1, wherein said transferring comprises issuing a memory copy write command over the communication link.</p> <p>3. The method of claim 1, wherein said transferring comprises issuing a command packet from the local node to the remote node over the communication link, the command packet containing the merged data.</p> <p>4. The method of claim 1, further comprising writing the merged data into a corresponding cache line of said another cache memory at the remote node.</p>	<p>What is claimed is:</p> <p>1. A massively parallel processing system, comprising:</p> <p>an interconnect network;</p> <p>a plurality of processing nodes, wherein each processing node includes:</p> <p>a processor;</p> <p>local memory;</p> <p>2. The system according to claim 1 wherein one of the local memories includes a first memory location and wherein the router circuit further includes an external registers circuit, wherein the external registers circuit includes:</p> <p>a plurality of external registers connected to the processor via a data bus;</p> <p>an address translator for calculating, based on an index written to the data bus, an address associated with the first memory location; and</p> <p>transfer means, connected to the plurality of external registers, for transferring data between the first memory location and one of the plurality of external registers.</p> <p>3. The system according to claim 2 wherein the router circuit further includes an integrated address centrifuge.</p> <p>4. The system according to claim 1 wherein the I/O routing means includes means for forwarding to the I/O controller a message packet received by the router circuit.</p>

In addition to the '738 patent, M•CAM DOORS™ has identified other documents in the innovation space that may contain critical elements of enabling technologies that predate key aspects of the innovations described in the claims of RE40877 and may be of material importance to discussions around 3PAR's acquisition. For a sample list of these findings, please see Appendix 1.

Public Domain Alternatives

Many patents in the public domain go unconsidered and unnoticed by businesses. Incorporating public domain technologies into product development strategies can give existing research and development initiatives a head-start with no additional investment, provide cost savings over proprietary alternatives, minimize licensing costs, stimulate overall innovation in this technology area and offer an avenue free of costly patent litigation suits. M•CAM DOORS™, has identified many patents which may provide public domain alternatives to RE40877, a sampling of which is included below.

Sample of Public Domain Patent Holdings related to data storage systems:

<u>Document #</u>	<u>Title</u>	<u>Assignee Name</u>	<u>Priority</u>	<u>File</u>	<u>Issue</u>
US 7,069,545	Quantization and compression for computation reuse	Intel Corporation	29-Dec-00	29-Dec-00	27-Jun-06
US 7,055,172	Problem determination method suitable for use when a filter blocks SNMP access to network components	International Business Machines Corporation	8-Aug-02	8-Aug-02	30-May-06
US 7,024,613	Method and apparatus for implementing infiniband transmit queue	International Business Machines Corporation	6-Feb-03	6-Feb-03	4-Apr-06
US 6,904,040	Packet preprocessing interface for multiprocessor network handler	International Business Machines Corporaiton	5-Oct-01	5-Oct-01	7-Jun-05
US 6,549,989	Extended cache coherency protocol with a "lock released" state	International Business Machines Corporation	9-Nov-99	9-Nov-99	15-Apr-03
US 6,173,361	Disk control device adapted to reduce a number of access to disk devices and method thereof	Fujitsu Limited	19-Jan-98	22-May-98	9-Jan-01
US 6,061,739	Network address assignment using physical address resolution protocols	International Business Machines Corp.	26-Nov-97	26-Nov-97	9-May-00
US 6,044,438	Memory controller for controlling memory accesses across networks in distributed shared memory processing systems	International Business Machiness Corporation	10-Jul-97	10-Jul-97	28-Mar-00
US 5,787,477	Multi-processor cache coherency protocol allowing asynchronous modification of cache data	International Business Machines Corporation	18-Jun-96	18-Jun-96	28-Jul-98
US 5,687,342	Memory range detector and translator	NCR Corporation	18-Sep-91	18-Sep-91	11-Nov-97
US 5,592,225	Device and method for controlling coding	Matsushita Electric Industrial Co., Ltd.	30-Sep-93	28-Sep-94	7-Jan-97
US 5,535,366	Method of and circuit arrangement for freeing communications resources, particularly for use by a switching element	Alcatel N. V.	12-Mar-90	6-Mar-91	9-Jul-96
US 5,353,412	Partition control circuit for separately controlling message sending of nodes of tree-shaped routing network to divide the network into a number of partitions	Thinking Machines Corporation	3-Oct-90	16-Aug-91	4-Oct-94
US 5,125,093	Interrupt control for multiprocessor computer system	Nexgen Microsystems	14-Aug-90	14-Aug-90	23-Jun-92
US 5,081,575	Highly parallel computer architecture employing crossbar switch with selectable pipeline delay	Oryx Corporation	6-Nov-87	3-May-89	14-Jan-92
AU2002231167	Method of "split-brain" prevention in computer cluster systems	EMC CORP	21-Dec-00	19-Dec-01	6-Oct-05

Conclusion

M•CAM’s intellectual property analysis has identified several examples of un-cited prior art that may limit the strength and defensibility of 3PAR’s U.S. Pat No. RE40877, some of which are held by Hewlett-Packard, itself. Ironically, HP has a history of purchasing its own invalidating prior art through its various acquisitions (think about their massive abandonment of COMPAQ assets after another acquisition).

A number of other large entities in addition to HP are also present in this innovation space with their own patent positions. The unprecedented scale of this bidding war has brought 3PAR into the public eye and will lead other companies to further scrutinize these innovations that went for such a high price. By bringing 3PAR’s intellectual property into HP, the litigation risk to HP has gone through the roof – an observation that is not currently priced into the market.

Appendix 1

Samples of Precedent Innovation:

<u>Document #</u>	<u>Title</u>	<u>Assignee Name</u>	<u>Priority</u>	<u>File</u>	<u>Issue</u>
US 6,148,349	Dynamic and consistent naming of fabric attached storage by a file system on a compute node storing information mapping API system I/O calls for data objects with a globally unique identification	NCR Corporation	24-May-96	6-Feb-98	14-Nov-00
US 6,108,812	Target device XOR engine	LSI Logic Corporation	20-Jun-96	20-Jun-96	22-Aug-00
US 6,073,211	Method and system for memory updates within a multiprocessor data processing system	International Business Machines Corporation	13-Dec-94	18-Apr-97	6-Jun-00
US 6,058,421	Method and system for addressing network host interfaces from a cable modem using DHCP	3Com Corporation	4-Feb-98	4-Feb-98	2-May-00
US 6,049,476	High memory capacity DIMM with data and state memory	Silicon Graphics, Inc.	15-May-95	31-Jul-98	11-Apr-00
US 6,032,266	Network system having function of changing route upon failure	Hitachi, Ltd.	5-Apr-96	3-Apr-97	29-Feb-00
US 6,014,383	System and method for controlling multiple initiators in a fibre channel environment	Compaq Computer Corporation	10-Feb-97	10-Feb-97	11-Jan-00
US 5,991,893	Virtually reliable shared memory	Hewlett-Packard Company	29-Aug-97	29-Aug-97	23-Nov-99
US 5,991,308	Lower overhead method for data transmission using ATM and SCDMA over hybrid fiber coax cable plant	Terayon Communication Systems, Inc.	25-Aug-95	4-Dec-96	23-Nov-99
US 5,990,852	Display screen duplication system and method	Fujitsu Limited	31-Oct-96	31-Oct-96	23-Nov-99
US 5,982,697	Method for initializing and reprogramming a control operation feature of a memory device	Micron Technology, Inc.	2-Dec-96	20-Mar-98	9-Nov-99
US 5,974,514	Controlling SDRAM memory by using truncated burst read-modify-write memory operations	Hewlett-Packard	12-Nov-96	12-Nov-96	26-Oct-99
US 5,964,891	Diagnostic system for a distributed data access networked system	Hewlett-Packard Company	27-Aug-97	27-Aug-97	12-Oct-99
US 5,958,009	System and method for efficiently monitoring quality of service in a distributed processing environment	Hewlett-Packard Company	27-Feb-97	27-Feb-97	28-Sep-99
US 5,923,840	Method of reporting errors by a hardware element of a distributed computer system	International Business Machines Corporation	8-Apr-97	8-Apr-97	13-Jul-99
US 5,900,015	System and method for maintaining cache coherency using path directories	International Business Machines Corporation	9-Aug-96	9-Aug-96	4-May-99
US 5,886,643	Method and apparatus for discovering network topology	Concord Communications Incorporated	17-Sep-96	17-Sep-96	23-Mar-99
US 5,878,420	Network monitoring and management system	Compuware Corporation	31-Aug-95	29-Oct-97	2-Mar-99
US 5,864,738	Massively parallel processing system using two data paths: one connecting router circuit to the interconnect network and the other connecting router circuit to I/O controller	Cray Research, Inc.	13-Mar-96	13-Mar-96	26-Jan-99
US 5,864,671	Hybrid memory access protocol for servicing memory access request by ascertaining whether the memory block is currently cached in determining which protocols to be used	Sun Microsystems, Inc.	1-Jul-96	1-Jul-96	26-Jan-99
US 5,860,159	Multiprocessing system including an apparatus for optimizing spin--lock operations	Sun Microsystems, Inc.	1-Jul-96	1-Jul-96	12-Jan-99
US 5,796,939	High frequency sampling of processor performance counters	Digital Equipment Corporation	10-Mar-97	10-Mar-97	18-Aug-98

Samples of Concurrent Innovation:

<u>Document #</u>	<u>Title</u>	<u>Assignee Name</u>	<u>Priority</u>	<u>File</u>	<u>Issue</u>
US 7,788,452	Method and apparatus for tracking cached addresses for maintaining cache coherency in a computer system having multiple caches	International Business Machines Corporation	20-Jan-04	20-Jan-04	31-Aug-10
US 7,747,717	Fast application notification in a clustered computing system	Oracle International Corporation	14-Aug-03	12-Aug-04	29-Jun-10
US 7,739,380	System and method for distributed management of shared computers	Microsoft Corporation	24-Oct-00	12-Nov-04	15-Jun-10
US 7,716,673	Tasks distribution in a multi-processor including a translation lookaside buffer shared between processors	Texas Instruments Incorporated	31-Jul-02	31-Jul-03	11-May-10
US 7,711,121	System and method for distributed management of shared computers	Microsoft Corporation	24-Oct-00	2-Nov-04	4-May-10
US 7,694,065	Distributed cache architecture	SAP AG	28-Dec-04	28-Dec-04	6-Apr-10
US 7,689,660	Application server architecture	SAP AG	9-Jun-05	9-Jun-05	30-Mar-10
US 7,684,964	Model and system state synchronization	Microsoft Corporation	6-Mar-03	8-Sep-05	23-Mar-10
US 7,684,401	Method and system for using extended fabric features with fibre channel switch elements	QLOGIC, Corporation	21-Jul-03	20-Jul-04	23-Mar-10
US 7,681,242	Allocation of network resources	Novell, Inc.	26-Aug-04	26-Aug-04	16-Mar-10
US 7,664,847	Managing workload by service	Oracle International Corporation	14-Aug-03	12-Aug-04	16-Feb-10
US 7,664,018	Methods and apparatus for switching fibre channel arbitrated loop devices	Emulex Design & Manufacturing Corporation	2-Jul-02	1-Jul-03	16-Feb-10
US 7,644,161	Topology for a hierarchy of control plug-ins used in a control system	Hewlett-Packard Development Company, L.P.	28-Jan-05	28-Jan-05	5-Jan-10
US 7,636,917	Network load balancing with host status information	Microsoft Corporation	30-Jun-03	30-Jun-03	22-Dec-09
US 7,630,384	Method and system for distributing credit in fibre channel systems	QLOGIC, Corporation	21-Jul-03	20-Jul-04	8-Dec-09
US 7,630,300	Methods and apparatus for trunking in fibre channel arbitrated loop systems	Emulex Design & Manufacturing Corporation	2-Jul-02	10-Jul-03	8-Dec-09
US 7,620,059	Method and apparatus for accelerating receive-modify-send frames in a fibre channel network	QLOGIC, Corporation	16-Jul-03	12-Jul-04	17-Nov-09
US 7,613,866	Method for controlling access to a multibank memory	Thomson Licensing	2-Sep-03	10-Aug-04	3-Nov-09
US 7,613,822	Network load balancing with session information	Microsoft Corporation	30-Jun-03	30-Jun-03	3-Nov-09
US 7,606,929	Network load balancing with connection manipulation	Microsoft Corporation	30-Jun-03	8-Sep-03	20-Oct-09
US 7,606,898	System and method for distributed management of shared computers	Microsoft Corporation	24-Oct-00	24-Oct-00	20-Oct-09
US 7,580,999	Remote system administration and seamless service integration of a data communication network management system	Cisco Technology, Inc.	4-Jan-99	8-Oct-03	25-Aug-09
US 7,580,354	Multi-speed cut through operation in fibre channel switches	QLOGIC, Corporation	21-Jul-03	20-Jul-04	25-Aug-09
US 7,574,708	Mechanism for enabling the distribution of operating system resources in a multi-node computer system	International Business Machines Corporation	4-Mar-04	4-Mar-04	11-Aug-09
US 7,573,909	Method and system for programmable data dependant network routing	QLOGIC, Corporation	21-Jul-03	20-Jul-04	11-Aug-09
US 7,594,111	Secure execution of a computer program	Massachusetts Institute of Technology	19-Dec-02	18-Dec-03	22-Sep-09
US 7,593,997	Method and system for LUN remapping in fibre channel networks	QLOGIC, Corporation	1-Oct-04	1-Oct-04	22-Sep-09
US 7,593,930	Fast channel architecture	SAP AG	14-Dec-04	14-Dec-04	22-Sep-09
US 7,591,006	Security for external system management	SAP AG	29-Dec-04	29-Dec-04	15-Sep-09
US 7,590,736	Flexible network load balancing	Microsoft Corporation	30-Jun-03	30-Jun-03	15-Sep-09
US 7,583,597	Method and system for improving bandwidth and reducing idles in fibre channel switches	Qlogic Corporation	21-Jul-03	20-Jul-04	1-Sep-09

M•CAM's Patent Glossary

<u>Aligned Sector:</u>	The business sector in which the product(s) resulting from the patent(s) is currently or intended to be sold.
<u>Applicant:</u>	The person or corporation that applies for a patent with the intent to use, manufacture or license the technology of the invention; under U.S. law, except in special situations, the applicant(s) must be the inventor(s).
<u>Application:</u>	Complete papers submitted to the U. S. Patent and Trademark Office seeking a patent including oath, specification, claims, and drawings. This usually does not signify a Provisional Patent Application, but only a regular patent application.
<u>Art:</u>	The established practice and public knowledge within a given field of technology. This also identifies a process or method used to produce a useful result. A term used in consideration of the problem of patentable novelty encompassing all that is known prior to the filing date of the application in the particular field of the invention.
<u>Assignee:</u>	The person(s) or corporate body to whom the law grants or vests a patent right. This refers to the person or corporate entity that is identified as the receiver of an assignment.
<u>Business Method</u>	
<u>Patent:</u>	A patent that controls the way a business process is undertaken. The issuance of these patents by the United States Patent and Trademark Office (USPTO) is new and controversial, since many allege that it is unfair to allow a patent on a way of doing business.
<u>Citation:</u>	This may include patents or journal articles that the applicant or examiner deems relevant to a current application. A reference to legal authorities or a prior art documentation are examples of a citation.
<u>Claim:</u>	The language in a patent application that defines the legal scope of the patent. Most patents have numerous claims. This is typically the single most important section in the application.
<u>Concurrent Art:</u>	Concurrent art occurs when related patent applications are being examined by the USPTO at the same time. It is difficult for any company or inventor to know, at the time they file for a patent, whether a "related" patent application exists.
<u>Filing Date:</u>	The date when a properly prepared application reaches the patent office in complete form.
<u>Innovation Cycle:</u>	A description of the commercialization timeframe for the intellectual property.
<u>Innovation Space:</u>	M•CAM's representation of the innovation(s) that occur before, during, and after the pending period of the subject patent. The innovation space is the first place to look for patents that are closely related to the subject patent and that may impact the defensibility of the subject patent or create opportunities for patent licensing.
<u>Issue Date:</u>	Not to be confused with the filing date, which is the date the patent application was physically received by the U.S. Patent and Trademark Office. This is the date on which the patent actually issues.
<u>Non-Aligned</u>	
<u>Sector:</u>	Any sector in which the patent can be used or sold, other than the sector for which the patent or resultant product was invented or intended.
<u>Pod:</u>	A group of patents owned by a company that should be treated as a single unit of innovation (e.g., a certain group of patents that comprise a single product or multiple related products).
<u>Prior Art:</u>	Any relevant patent that was issued before the patent being analyzed. If this previous patent was specifically mentioned in the new patent's application, the previous patent is referred to as "cited prior art". If it was NOT mentioned, then that previous patent is referred to as "uncited prior art".
<u>Subsequent Art:</u>	Any patent that has a filing date with the USPTO that is after the issuance date of the subject patent. This subsequent art patent may or may not have cited (see "Citation" above) the subject patent. As subsequent art represents more recent innovation than the subject patent, it has great potential to shrink the market opportunity for the subject patent.

A Brief Primer on the Patent System

In recent years, the importance of patents and intellectual property rights as an important variable in the marketplace has come to the forefront of the public consciousness as world leaders declare their country's lead in the innovation race. Damaging intellectual property litigation is becoming increasingly common across all industries. This is exacerbated when patent rights are granted for non-novel ideas. A vast amount of precedent innovation is unconsidered by patent-granting authorities in the creation of new IP rights. Patent granting authorities including the United States Patent and Trademark Office (USPTO), European Patent Office (EPO), Japanese Patent Office (JPO), Chinese State Intellectual Property Office (SIPO), Korean Intellectual Property Office (KIPO) and many others are constrained by the use of patent classification systems which are routinely circumvented by patent applicants.

There is a two-way social contract underlying the patent system. In the United States, patent terms are generally limited to 20 years from the date of application. By statutory intention, once a patent has expired, the patent holder loses the right to exclude others from fully utilizing any innovation described in the patent. A large number of patents enter the public domain when they are "abandoned" – when owners discontinue paying patent maintenance fees. Patents also only provide an exclusionary right in the country for which the patent is filed. As demonstrated by the Global Innovation Commons¹ (G.I.C.), using intellectual property available in the public domain eliminates the need to pay licensing fees on those innovations in countries where the patent was never registered, or worldwide, if abandoned.

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¹ <http://www.globalinnovationcommons.org/>