Avago Technologies vs Maxim Integrated Products

Intellectual Property Analysis of Integrated Circuits

On April 23rd, 2015, Avago Technologies General IP (Singapore) PTE. LTD filed suit against Maxim Integrated Products, Inc. regarding their semiconductor devices. Avago claims that Maxim infringes on five patents (US 5,523,359; US 5,599,739; US 6,040,616; US 6,083,271; and US 6,194,323) when manufacturing its MAX6946, MAX2634, MAX7356, MAX17126, DS28E10, MAX1305, and other semiconductor products. Maxim had, for nearly two decades, licensed semiconductor technologies from LSI Corporation's patent portfolio. The license to these technologies lapsed on December 31, 2011. Avago acquired LSI in 2014, and claims that Maxim has continued to benefit from the technologies represented by the LSI portfolio. These technologies broadly cover methods for improved integrated circuit fabrication and design, including hard mask etching, barrier layer treatment, and specifying multiple power domains.

Analysis

Using our proprietary analytical systems, we looked at the Avago patents and assertion. We found that four of the asserted patents are severely impaired by precedent innovation. The technologies represented in the Avago assertion more than likely belong in a freedom-to-operate space, negating the need for a license to practice them.

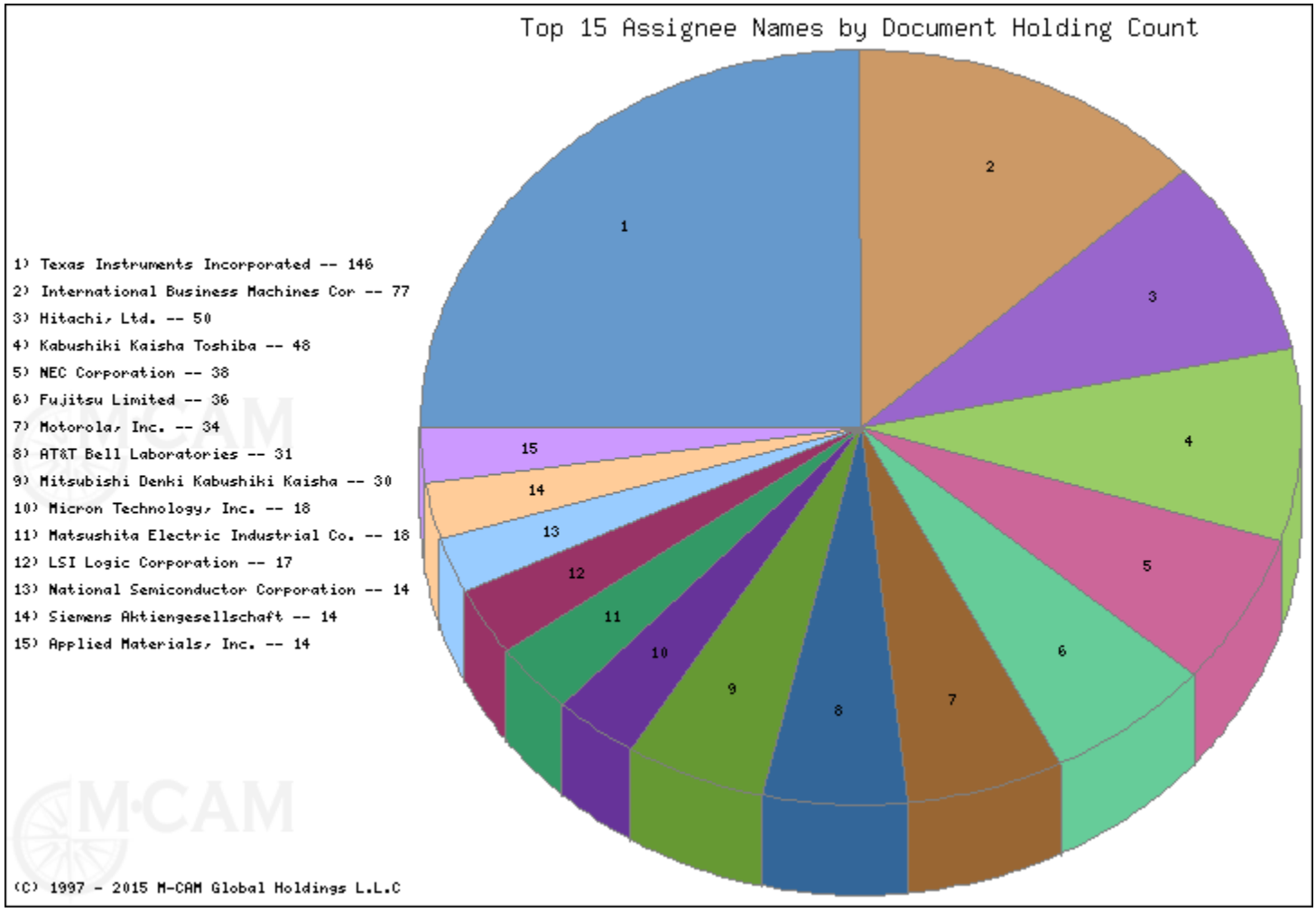
Below is a view of Avago's five asserted patents.

Document #	Title	Assignee Name	Priority	File	Issue
US6194323	Deep sub-micron metal etch with in-situ hard mask etch	Lucent Technologies Inc.	16-Dec-98	16-Dec-98	27-Feb-01
US6083271	Method and apparatus for specifying multiple power domains in electronic circuit designs	LSI Logic Corporation	5-May-98	5-May-98	4-Jul-00
US6040616	Device and method of forming a metal to metal capacitor within an integrated circuit	Lucent Technologies Inc.	6-Jun-95	12-Aug-97	21-Mar-00
US5599739	Barrier layer treatments for tungsten plug	Lucent Technologies Inc.	30-Dec-94	30-Dec-94	4-Feb-97
US5523259	Method of forming metal layers formed as a composite of sub-layers using Ti texture control layer	AT&T Corp.	5-Dec-94	5-Dec-94	4-Jun-96

Integrated Circuit Fabrication

The Avago patents occupy a well tread space in integrated circuit fabrication technology, and despite Maxim's earlier licensing of the LSI patent portfolio it is clear that the claimed infringement faces an uphill battle as the methods and processes described in the patents in suit are articulated in relevant precedent innovation.

The chart below shows other entities involved in the technology space of the Avago patents. These entities have all been operating in this technology space for a significant period of time. As you can see entitles such as Texas Instruments and IBM hold a large amount of patents in the integrated circuit fabrication, and thus we find significant overlap with the patents in suit.



Selected Precedent Innovation

The following tables show the precedent innovation for the Avago patents in suit.

Precedent Innovation for US 5,523,259

Document #	Title	Assignee Name	Priority	File	Issue
US5360524	Method for planarization of submicron vias and the manufacture of semiconductor integrated circuits	Rudi Hendel	13-Apr-93	13-Apr-93	1-Nov-94
US5358616	Filling of vias and contacts employing an aluminum-germanium alloy	Michael G. Ward	17-Feb-93	17-Feb-93	25-Oct-94
US5318923	Method for forming a metal wiring layer in a semiconductor device	Samsung Electronics Co. Ltd.	19-Sep-90	11-Jun-92	7-Jun-94
US5312772	Method of manufacturing interconnect metallization comprising metal nitride and silicide	Seiko Epson Corporation	6-Aug-88	1-Apr-92	17-May-94
US5288665	Process for forming low resistance aluminum plug in via electrically connected to overlying patterned metal layer for integrated circuit structures	Applied Materials, Inc.	12-Aug-92	12-Aug-92	22-Feb-94
US5270255	Metallization process for good metal step coverage while maintaining useful alignment mark	Chartered Semiconductor Manufacturing Pte, Ltd.	8-Jan-93	8-Jan-93	14-Dec-93
US5266521	Method for forming a planarized composite metal layer in a semiconductor device	Samsung Electronics Co., Ltd.	20-Mar-91	31-Jan-92	30-Nov-93
US5242860	Method for the formation of tin barrier layer with preferential (111) crystallographic orientation	Applied Materials, Inc.	24-Jul-91	24-Jul-91	7-Sep-93
US5240880	Ti/TiN/Ti contact metallization	Zilog, Inc.	5-May-92	5-May-92	31-Aug-93
US5171412	Material deposition method for integrated circuit manufacturing	Applied Materials, Inc.	23-Aug-91	23-Aug-91	15-Dec-92
US5108570	Multistep sputtering process for forming aluminum layer over stepped semiconductor wafer	Applied Materials, Inc.	30-Mar-90	30-Mar-90	28-Apr-92
US5106781	Method of establishing an interconnection level on a semiconductor device having a high integration density	U.S. Philips Corporation	12-Jul-88	5-Nov-90	21-Apr-92
US5071714	Multilayered intermetallic connection for semiconductor devices	International Business Machines Corporation	17-Apr-89	17-Apr-89	10-Dec-91
US5049975	Multi-layered interconnection structure for a semiconductor device	Mitsubishi Denki Kabushiki Kaisha	14-Mar-89	12-Mar-90	17-Sep-91
US4994162	Planarization method	Materials Research Corporation	29-Sep-89	29-Sep-89	19-Feb-91
US4960732	Contact plug and interconnect employing a barrier lining and a backfilled conductor material	Advanced Micro Devices, Inc.	19-Feb-87	14-Nov-89	2-Oct-90
US4944961	Deposition of metals on stepped surfaces	Rensselaer Polytechnic Institute	5-Aug-88	5-Aug-88	31-Jul-90
US4910580	Method for manufacturing a low-impedance, planar metallization composed of aluminum or of an aluminum alloy	Siemens Aktiengesellschaft	27-Aug-87	1-Aug-88	20-Mar-90

Precedent Innovation for US 5,599,739

Document #	Title	Assignee Name	Priority	File	Issue
US4897709	Titanium nitride film in contact hole with large aspect ratio	Hitachi, Ltd.	15-Apr-88	26-May-88	30-Jan-90
US5371042	Method of filling contacts in semiconductor devices	Applied Materials, Inc.	16-Jun-92	16-Jun-92	6-Dec-94
US5306666	Process for forming a thin metal film by chemical vapor deposition	Nippon Steel Corporation	24-Jul-92	21-Jul-93	26-Apr-94
US5278448	Semiconductor device and method of fabricating the same	Matsushita Electric Industrial Co., Ltd.	19-Mar-91	18-Mar-92	11-Jan-94
US5242860	Method for the formation of tin barrier layer with preferential (111) crystallographic orientation	Applied Materials, Inc.	24-Jul-91	24-Jul-91	7-Sep-93
US5094981	Technique for manufacturing interconnections for a semiconductor device by annealing layers of titanium and a barrier material above 550.degree. C .	North American Philips Corporation, Signetics Div.	17-Apr-90	17-Apr-90	10-Mar-92
US5084414	Metal interconnection system with a planar surface	Hewlett-Packard Company	15-Mar-85	27-Jul-90	28-Jan-92
US5036382	Semiconductor device having a multi-level wiring structure	Yamaha Corporation	22-Feb-89	21-Feb-90	30-Jul-91
US5008730	Contact stud structure for semiconductor devices	International Business Machines Corporation	3-Oct-88	18-Dec-89	16-Apr-91
US4990467	Method of preventing residue on an insulator layer in the fabrication of a semiconductor device	Samsung Electronics Co., Ltd.	11-Aug-88	12-Jul-89	5-Feb-91
US4970574	Electromigrationproof structure for multilayer wiring on a semiconductor device	NEC Corporation	31-May-88	31-May-89	13-Nov-90

Precedent Innovation for US 6,040,616

Document #	Title	Assignee Name	Priority	File	Issue
US5510651	Semiconductor device having a reducing/oxidizing conductive material	Motorola, Inc.	7-Jun-93	18-Nov-94	23-Apr-96
US5401680	Method for forming a ceramic oxide capacitor having barrier layers	National Semiconductor Corporation	18-Feb-92	18-Feb-92	28-Mar-95
US5304506	On chip decoupling capacitor	Micron Semiconductor, Inc.	10-Mar-93	10-Mar-93	19-Apr-94
US5191510	Use of palladium as an adhesion layer and as an electrode in ferroelectric memory devices	Ramtron International Corporation	29-Apr-92	29-Apr-92	2-Mar-93
US4638400	Refractory metal capacitor structures, particularly for analog integrated circuit devices	General Electric Company	24-Oct-85	24-Oct-85	20-Jan-87

Precedent Innovation for US 6,083,271

Document #	Title	Assignee Name	Priority	File	Issue
US5272645	Channel routing method	Matsushita Electric Industrial Co., Ltd.	24-May-90	22-May-91	21-Dec-93
US5519630	LSI automated design system	Matsushita Electric Industrial Co., Ltd.	22-Mar-93	21-Mar-94	21-May-96
US5084824	Simulation model generation from a physical data base of a combinatorial circuit	National Semiconductor Corporation	29-Mar-90	29-Mar-90	28-Jan-92
US5050091	Integrated electric design system with automatic constraint satisfaction	Electric Editor, Inc.	28-Feb-85	21-Aug-90	17-Sep-91
US4922432	Knowledge based method and apparatus for designing integrated circuits using functional specifications	International Chip Corporation	13-Jan-88	13-Jan-88	1-May-90
US4918614	Hierarchical floorplanner	LSI Logic Corporation	2-Jun-87	2-Jun-87	17-Apr-90
US4890238	Method for physical VLSI-chip design	International Business Machines Corporation	17-Dec-86	15-Dec-87	26-Dec-89
US4833619	Automatic logic design system	Hitachi, Ltd.	8-Jan-86	24-Dec-86	23-May-89
US4827427	Instantaneous incremental compiler for producing logic circuit designs	Stanley M. Hyduke	5-Mar-87	5-Mar-87	2-May-89
US4811237	Structured design method for generating a mesh power bus structure in high density layout of VLSI chips	General Electric Company	24-Jun-87	24-Jun-87	7-Mar-89
US4703435	Logic Synthesizer	International Business Machines Corporation	16-Jul-84	16-Jul-84	27-Oct-87

Precedent Innovation for US 6,194,323

Document #	Title	Assignee Name	Priority	File	Issue
US5930634	Method of making an IGFET with a multilevel gate	Advanced Micro Devices, Inc.	21-Apr-97	21-Apr-97	27-Jul-99

Our systems found that the Avago patents were granted from 1996-2001 while precedent innovation stretching as far back as the 1980's covers these technology areas. There is significant un-cited precedent innovation in the innovation space, calling Avago's claims of infringement into question.

For a more detailed examination of the patents mentioned in this report, please contact us at patentlyobvious@m-cam.com**.**

M·CAM's Patent Glossary

Aligned Sector: The business sector in which the product(s) resulting from the patent(s) is currently or intended to be sold.

Applicant: The person or corporation that applies for a patent with the intent to use, manufacture or license the technology of the invention; under U.S. law, except in special situations, the applicant(s) must be the inventor(s).

Application: Complete papers submitted to the U. S. Patent and Trademark Office seeking a patent including oath, specification, claims, and drawings. This usually does not signify a Provisional Patent Application, but only a regular patent application.

Art: The established practice and public knowledge within a given field of technology. This also identifies a process or method used to produce a useful result. A term used in consideration of the problem of patentable novelty encompassing all that is known prior to the filing date of the application in the particular field of the invention.

Assignee: The person(s) or corporate body to whom the law grants or vests a patent right. This refers to the person or corporate entity that is identified as the receiver of an assignment.

Business Method Patent: A patent that controls the way a business process is undertaken. The issuance of these patents by the United States Patent and Trademark Office (USPTO) is new and controversial, since many allege that it is unfair to allow a patent on a way of doing business.

Citation: This may include patents or journal articles that the applicant or examiner deems relevant to a current application. A reference to legal authorities or a prior art documentation are examples of a citation.

Claim: The language in a patent application that defines the legal scope of the patent. Most patents have numerous claims. This is typically the single most important section in the application.

Concurrent Art: Concurrent art occurs when related patent applications are being examined by the USPTO at the same time. It is difficult for any company or inventor to know, at the time they file for a patent, whether a "related" patent application exists.

Filing Date: The date when a properly prepared application reaches the patent office in complete form.

Innovation Cycle: A description of the commercialization timeframe for the intellectual property.

Innovation Space: M·CAM's representation of the innovation(s) that occur before, during, and after the pending period of the subject patent. The innovation space is the first place to look for patents that are closely related to the subject patent and that may impact the defensibility of the subject patent or create opportunities for patent licensing.

Issue Date: Not to be confused with the filing date, which is the date the patent application was physically received by the U.S. Patent and Trademark Office. This is the date on which the patent actually issues.

Non-Aligned Sector: Any sector in which the patent can be used or sold, other than the sector for which the patent or resultant product was invented or intended.

Pod: A group of patents owned by a company that should be treated as a single unit of innovation (e.g., a certain group of patents that comprise a single product or multiple related products).

Prior Art: Any relevant patent that was issued before the patent being analyzed. If this previous patent was specifically mentioned in the new patent's application, the previous patent is referred to as "cited prior art". If it was NOT mentioned, then that previous patent is referred to as "uncited prior art".

Subsequent Art: Any patent that has a filing date with the USPTO that is after the issuance date of the subject patent. This subsequent art patent may or may not have cited (see "Citation" above) the subject patent. As subsequent art represents more recent innovation than the subject patent, it has great potential to shrink the market opportunity for the subject patent.

A Brief Primer on the Patent System

In recent years, the importance of patents and intellectual property rights as an important variable in the marketplace has come to the forefront of the public consciousness as world leaders declare their country's lead in the innovation race. Damaging intellectual property litigation is becoming increasingly common across all industries. This is exacerbated when patent rights are granted for non-novel ideas. A vast amount of precedent innovation is unconsidered by patent-granting authorities in the creation of new IP rights. Patent granting authorities including the United States Patent and Trademark Office (USPTO), European Patent Office (EPO), Japanese Patent Office (JPO), Chinese State Intellectual Property Office (SIPO), Korean Intellectual Property Office (KIPO) and many others are constrained by the use of patent classification systems which are routinely circumvented by patent applicants.

There is a two-way social contract underlying the patent system. In the United States, patent terms are generally limited to 20 years from the date of application. By statutory intention, once a patent has expired, the patent holder loses the right to exclude others from fully utilizing any innovation described in the patent. A large number of patents enter the public domain when they are "abandoned" – when owners discontinue paying patent maintenance fees. Patents also only provide an exclusionary right in the country for which the patent is filed. As demonstrated by the Global Innovation Commons[1] (G.I.C.), using intellectual property available in the public domain eliminates the need to pay licensing fees on those innovations in countries where the patent was never registered, or worldwide, if abandoned.

Patently Obvious® is a weekly report focusing on select groups of patents in order to increase transparency in markets, addressing information asymmetries, and providing a more level playing field for all parties.

[1] http://www.globalinnovationcommons.org/